An SIC Bit Flipping Linear Feedback Shift Register for Low Power BIST

Sabir Hussain¹ and P H S T Murthy²
¹Assistant Professor, ECE Department, M J College of Engineering and Technology, Hyderabad.
²Assistant Professor, ECED Department, GITAM University, Vishakhapatnam, India.

Abstract— This paper presents low power BIST architecture using a modified low transition test pattern generator. We combined single input change (SIC) with Bit Flipping linear feedback shift register called SIC-BF LFSR. The proposed SIC-BF test pattern generator reduces the switching activity among the test patterns at the most. In the proposed design, the single input change generated by a m bit counter and a gray code generator are Ex-OR with the seed generated by the Bit Flipping linear feedback shift register. In this proposed method we tested digital circuit having 36-bit input and 7-bit output ISCAS’85 a 27-channel interrupt controller. It is verified from the results that the power consumed by CUT compared to existing LSA-TPG techniques reduced by 5.41%.

Keywords – Low power BIST, SIC-BS LFSR, Switching Transitions, ISCAS Benchmark circuits

I. INTRODUCTION

With the increase in the size and complexity of the Chip, the test vectors needed to test them has also increased which results in more power consumption. Due to the increased power consumption testing them has become a difficult problem Automatic test pattern generation (ATPG) the traditional test technique, uses software to target single faults for digital circuit testing have become expensive and can no longer provide sufficiently high fault coverage for deep submicron or nanometre designs from the chip point to the board and system point. Currently in IC technology, the conventional testing have become expensive and unsuccessful because highly complex chips have low accessibility of internal nodes. Built-in self test (BIST) is another approach to ease these testing problems where features of BIST are integrated into a digital circuit at the design level. Circuits that generate test vectors and analyze the output responses of the functional circuitry are implanted in the chip or elsewhere along with logic BIST, on the same board. In order to reduce the overall power consumption of the BIST circuitry proper design of the test pattern generator plays an important role.

Test Pattern Generators (TPG) test the IC in the most definitive and systematic way. TPG is the process which generates random test vectors which are distinctive and unrepeated. The most often used test pattern generator for generating different test vectors is linear feedback shift register (LFSR). To minimize the overall power dissipation while testing the CUT the correlations between these test vectors are lowered by using different techniques in the LFSRs. In general, the power dissipation of a system in test mode is more than normal mode [3]. Four reasons are blamed for power increase during test. The high transition activity, Due to shortage of at-speed equipment’s, Power consumed by additional testing circuitry and Low correlation among test vectors [4].

The extra power consumption creates problems such as increase in production cost, circuit reliability is reduced verification of performance will be difficult, portable systems will be dependent, and overall performance is reduced. Therefore different methods are presented in the literature to control the overall consumption of power. The novelty of our design is Ex-ORing the pattern generated by BF LFSR and SIC generator, we achieved significant reduction in transitions compared to conventional methods. The rest of the paper is structured as follows. In section II, Prior work applicable to minimizing the power are discussed, it mostly concentrates to lower the power consumption. In section III, Basic BIST architecture, an analysis of power dissipation for testing is presented and ISCAS Benchmark Circuit C432 a 27-channel interrupt controller is discussed briefly, which is the circuit under test (CUT) to verify the potency of the proposed method. In section IV proposed method which is a low power test pattern generator is discussed in detail. In Section V, the implementations details are discussed. Section VI outlines the conclusion.

II. PRIOR WORK

Different techniques are available to reduce the switching activities of test vectors; with the help of these methods the power in test mode can be reduced. A Novel BIST Scheme for Low Power Testing by Bo YE Tian-wang Li proposed LSA-TPG in [1] by using linear feedback shift register (LFSR) combination with SIC generators. A modified clock scheme was proposed by Patrick Girard in which only half of the D flip-flops works, therefore only half of the test vectors are switched [7]. A BIST TPG for low switching activity was proposed by S.K. Gupta in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. To reduce consumption of power by circuit during test LT-TPG is proposed [6]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR). A desirable low power can be achieved by using single input change pattern generators. To generate random single input change sequences a proposed method which is the combination of LFSR and scan shift register is used [9 &10]. In [11 &12], it is proposed that \((2^m-1)\) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, \(m\) is length of LFSR. In [5], it is proposed that \(2^m\) single input changing data is inserted between two neighbouring seeds. By using the above methods power consumptions is reduced, still the switching activities will
be large when clock frequency is high. This paper proposed a new technique to reduce switching activity with negligible clock frequency with compared to existing method.

III. BACKGROUND

Power consumption in CMOS circuits can be classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. Dynamic dissipation is due to short circuit current which is due to the transistors remaining in on state for small period of time and the charging and discharging of load capacitance during output switching. The most supreme source of power consumption in the present CMOS technology is dynamic power, this may also vary for upcoming improvements of high scaled CMOS circuits. The generalized expression for the switching power dissipation of a CMOS VLSI circuits can be calculated from the given equation [9].

\[ P = \alpha T \text{Load} V^2 \text{ad} f_{\text{clk}} \quad \text{(1)} \]

Where the switching activity is given by \( \alpha T \). The total load capacitance is represented by \( C_{\text{load}} \). The supply voltage is given by \( V_{\text{dd}} \) and the operating frequency is represented by \( f_{\text{clk}} \). The dynamic power consumed is directly proportional to the switching activity factor of the gate \( \alpha T \). By controlling the switching activity factor of the gate and the load capacitance the power dissipation during testing can be reduced. There are three parameters are important for evaluating the power properties of a system under test

A. Basic BIST Architecture:

In VLSI circuit design, BIST architecture is mainly used for testing. The primary goal of BIST is to reduce the power dissipation without degrading the overall system performance and fault coverage [3]. In order to reduce the costs of external circuit testing BIST has now become an alternative solution. The BIST approach promises to find greater use in a wide variety of circumstances as more and better BIST techniques are developed.

B. Design of C432 Benchmark circuit

We used C432 is a 27-channel interrupt controller as circuit under test (CUT). It consists of three 9 bit buses named as P, Q, R which represent the input channels. The bit position in each bus represents the priority of interrupt request. The interrupt requests are enabled and disabled by an additional 9-bit input bus (called E) in the respective bit positions. The figure below represents the circuit. It consists of 5 modules named F1, F2, F3, F4,and F5, which contain the underlying logic.

Three interrupt request buses P, Q and R are present in the interrupt controller, each having one channel-enable bus E and nine bits or channels. The Priority rules are applied as follows: for any x, y, z; P[x] > Q[y] > R[z], i.e., bus P has the high level priority and bus R the low level priority. The channel within each bus, with a higher index has priority over the one with a lower index; for illustration, P[x] > P[y], if x > y. If E[x] = 0, then the P[x], Q[x], and R[x] inputs are disregarded.

![Figure 2: C432 benchmark circuit](image)

It has seven outputs namely SP, SQ, SR and Chan [3:0]. Interrupt requests requested by the channel are acknowledged by these outputs. Only the channel of high level priority in the requesting bus of high level priority is acknowledged. One exception is that if two or more interrupts produce requests on the channel that is acknowledged, each bus is acknowledged. For illustration, if P[4], P[2], Q[6] and R[4] have requests pending, P[4] and R[4] are acknowledged. Module F5 is a 9-line-to-4-line priority encoder.

IV. PROPOSED LOW POWER TPG

A. Generating Test Vectors by using LFSR

The low power LFSR, which is the most widely used test pattern generator because of its small circuit area and excellent random characteristics. An n-stage standard LFSR consists of n-D flip-flops and a selected number of exclusive-OR (XOR) gates where XOR gates are placed on the external feedback path is also referred to as an external-XOR LFSR. A primitive polynomial of degree n over Galois field GF(2), p(x), as a polynomial that divides 1 + x^i, but not 1 + x^i, for any integer i < T, where T = 2^n-1. So
we are using a primitive polynomial based external XOR LFSR to generate the test patterns or test sequences for \( n = 36 \) the Primitive Polynomial is \( 1 + x^{24} + x^{35} \).

**B. Generating Test Vectors using SIC BF –LFSR**

The most widely used as test pattern generator is LFSR because of its small circuit area and excellent random characteristics. Bit Flipping is used as the seed generator in this paper. As shown in Fig. 2, the proposed architecture which is called SIC BF LFSR consists of a seed generator (BF), a counter of \( n \)-bit, a gray code converter and an EX-OR array. The \( n \)-bit counter and gray encoder generate used to generate single input changing patterns.

**Figure 3: Test Pattern Generator Circuit**

Gray encoder is used to encode the counter’s output \( C[n-1:0] \) so that two successive values of its output \( GC[n-1:0] \) will differ in only one bit. Gray code converter is implemented as follows.

- \( GC[0] = C[0] XOR C[1] \)
- \( GC[n-1] = C[n-1] \)

The seed generator circuit BF is modified LFSR structure to apply flipping between the neighbouring bits. For the flipping process the last bit is used as the selection line. If the last bit is ‘0’, then flipping is performed, else nothing will change.

The final test patterns are obtained as follows

\[
SG[0] = BS[0] XOR GC[0] \\
\vdots \\
SG[n-1] = BS[n-1] XOR GC[n-1]
\]

Due to the control signal the seed generator clock will be TCK/2m. The XOR output of the sequences and a certain vector must be a single input changing sequence because SICG’s cyclic sequences are single input changing patterns. The SIC generator shown in Fig. 4 is an example of counter and gray encoder’s output when \( n = 5 \) and \( m = 4 \). The seed does not change in a cycle when \( C[4:0] = 00000 \), and it will only switch to another vector when \( C[4:0] = 10000 \). It can be found that all values of GC[4:0] are single input changing patterns.

**Figure 4: 5 bit Gray code encoder**

An example of 5 bit single input changing sequence with the seed BS0 “00000” and with the seed BS1 “00100” when \( n = 5 \) and \( m = 4 \). The period of the single input changing sequences will be 16. 5 is a 5 bit single input changing sequence 5-bit gray encoder output sequence in Fig. 5 is \( \{00000, 00001, 00011, 00010, 00110, 00111, 00101, 01000, \ldots, 10000\} \). The chosen seeds BS0 and BS1 are \{00000\} and \{00100\}.

BS0 will be exclusive-ORed with sequence \( \{0000, 00001, 00011, 00010, 00110, 00111, 00101, 01000, \ldots, 10000\} \) and generates the SICG single input changing sequence \( \{0000, 00001, 00011, 00010, 00110, 00111, 00101, \ldots, 01000\} \).

BS1 will be exclusive-ORed with sequence \( \{11000, 11001, 11011, 11010, 11110, 11111, 11110, 11001, \ldots, 10000\} \) and generates the SICG single input changing sequence \( \{11000, 11001, 11011, 11010, 11110, 11111, 11110, 11001, \ldots, 10100\} \).

**Figure 5: Single input change generator circuit**

For illustration, two well-chosen seeds generate two single input changing sequences which are distinctive. The SICG circuit in Fig. 4 consists of a counter of \( n \) bits and a gray code converter. The counter of \( n \) bits consists of \( n \) D flip-flops and the gray code converter consists of \( n \)-l exclusive-OR gates. Under reasonable scope the hardware...
overhead can be controlled and the power consumption can be greatly reduced and it also guarantee the fault coverage. It is applicable for large scale circuits especially for System on chip.

V. IMPLEMENTATION DETAILS

To validate the effectiveness of the proposed method compared with LSA-TPG proposed in [1] A Novel BIST Scheme for Low Power Testing by Bo YE Tian-wang Li used LFSR combined with SIC LFSR. We select Test pattern generator (TPG) using conventional linear feedback shift register combined with Bit Flipping LFSR. The comparison results explain in table I shows the total power consumed by CUT ISCAS’85 Benchmark Circuit C432.

<table>
<thead>
<tr>
<th>Pattern Generators</th>
<th>Total Power consumed by CUT C432(mw)</th>
<th>Saving (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LFSR[1]</td>
<td>1.629</td>
<td>-----</td>
</tr>
<tr>
<td>LSA-TPG[1]</td>
<td>0.188</td>
<td>88.45</td>
</tr>
<tr>
<td>Proposed</td>
<td>0.100</td>
<td>93.86</td>
</tr>
</tbody>
</table>

The results obtained from the Xilinx 14.5 implementation with the device xc3s200-4pq208 targeted on Spartan 3E in which we have generated VCD file after the post simulation. X Power analyzer tool was used for the Power analysis, this analyzer takes certain input files viz .ncd file, pcf file and .vcd file for analysis. These files have been generated and supplied to the Xpower analyzer tool of the Xilinx 14.5 ISE.

VI. CONCLUSION

A modified SIC BF linear feedback shift registers. Which itself is a low power test pattern generator has been proposed in which the seed generated from BF is Ex-ORed with the single input changing sequences generated from gray code converter. This method adequately and effectively reduces the switching correlations among the test patterns. It greatly reducing the power consumption during testing mode with minimum number of switching correlations and gives better power reduction compared to the existing method. It is verified from the results that power reduced by the proposed method is by 5.41%.

REFERENCES
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